# Jisu Kwon

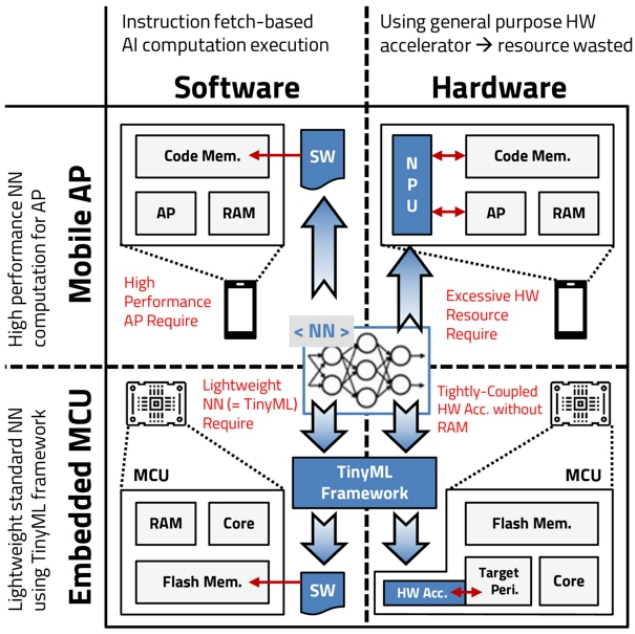
kjisu96@knu.ac.kr +82-(0)53-940-8648
Google Scholar LinkedIn My homepage
Kyungpook National University
School of Electronic and Electrical Engineering, College of IT
80 Daehak-ro, Buk-gu, Daegu, South Korea
IT1-724


Welcome!

## Research Interests

My research focuses on realizing AI at the edge, specifically addressing the challenge of executing neural network computations encompassing training and inference on MCUs. I have conducted **full-stack research aimed at improving the software for AI applications optimized for target MCU architectures and designing hardware architectures capable of efficiently executing embedded software**, including ARM core-based MCU HW/FW/SW/OS:

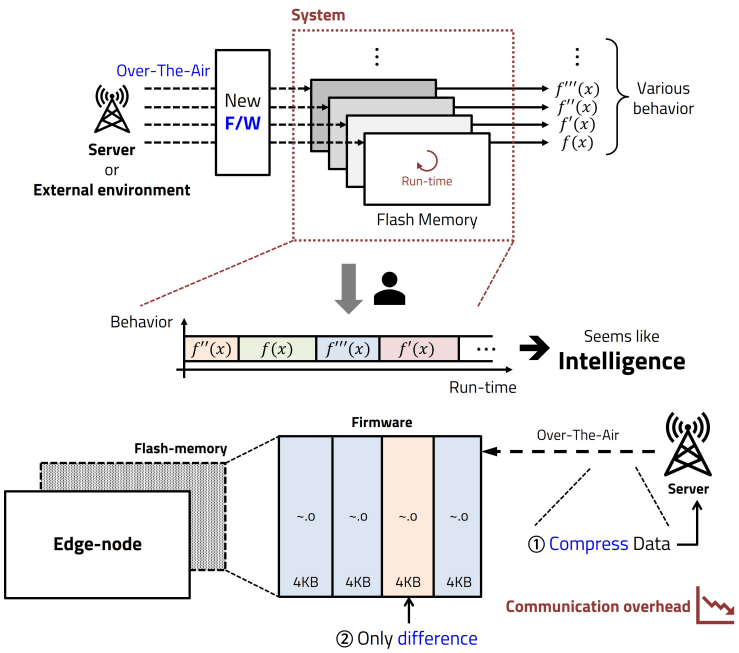
- ARM-core compatible physical chip & accelerator design.
- AMBA connectable RTL IP development & top integration.
- Efficient MCU firmware update technique development (STM32, Nordic NRF).
- Efficient OS-driven firmware design using automotive MCU (Infineon TriCore).
- Efficient chip verification platform using RTL simulator & system emulator-mixed framework.




**[Overview] Lightweight AI Acceleration on the Edge Devices**

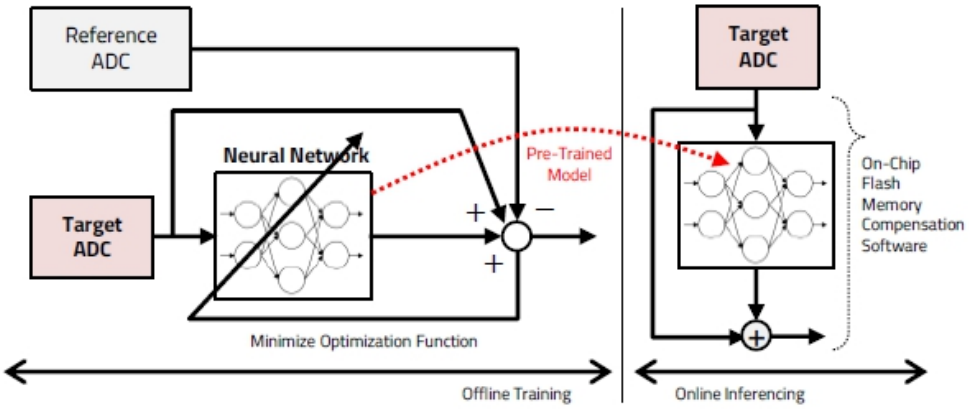
My research interests in AI on the embedded system by hardware & software co-design for lightweight edge AI. Typical inference requires only read operation to access static pre-trained weight parameters. On the other hand, training needs to use both read and write operations to update weight during backpropagation. In the case of MCU, on-device training faces two challenges; low-cost read-write accessible on-chip SRAM is too small to store the weight, and the relatively large flash memory has a write access constraint. Furthermore, considering conventional network size, flash memory is inevitable to realize on-device training on tiny MCU. To cope with the MCU memory constraints, we need to design AI software algorithms considering MCU hardware characteristics.

## Research Interests (continued)




**[FW] Efficient Microcontroller Firmware Update**

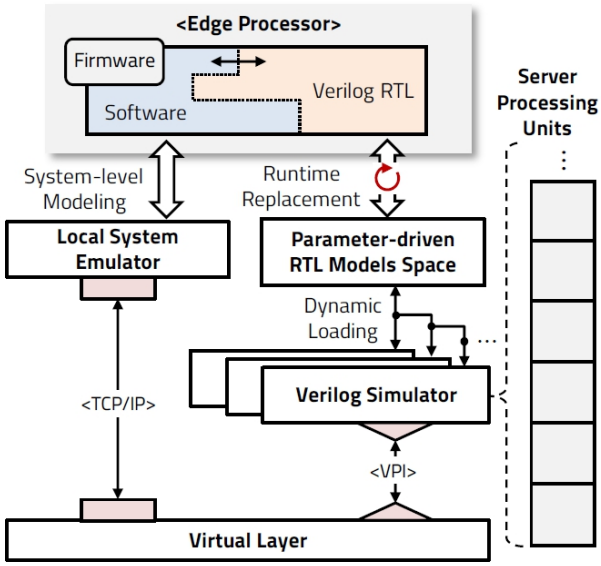
In applications where firmware updates are frequent, such as edge devices in the Internet of Things (IoT) networks with embedded systems, the update process is considered a significant role in improving device performance. This research proposed a user-insensible sliding firmware update technique based on a function block that reduces flash memory usage by handling only part of function blocks instead of the entire firmware, and the device's pause time by allowing the user to use the device between function block updates. The proposed technique was evaluated using the target board with the actual ARM core. We show that user-insensible sliding firmware update has great potential for implementing IoT networks that change behavior quickly by being aware of the environment.




**[HW, FW] Neural Network-based Hardware Compensation (ADC, ...)**

Typically, circuits had to be designed at a high cost to prevent irregular and random noise. This paper combines a low-cost designed part with a lightweight compensation technique, instead of designing a noise-tolerant circuit at a high cost. A technique that uses a compensate program in an embedded system has been applied to the ADC case study for compensating ADC output as ideal. The proposed technique implemented in embedded systems can compensate for deterministic noise operating on static hardware (ADC) as a minimal resource. The embedded system compensation technique can be applied to ADCs and various hardware that include human uninterpretable deterministic noise.

## Research Interests (continued)




**[HW, SW] Efficient SoC Verification using RTL Simulator & System Emulator-Mixed Platform**
Iterative register-transfer level (RTL) simulation is essential for the edge processor design, but the RTL simulation speed is significantly slower in a system where various RTL models are complicatedly integrated. The system emulator, which is written in a high-level language, and the Verilog simulation have different abstraction levels, thus the Verilog procedural interface (VPI) module is plugged into the Verilog simulator to connect with the virtual layer interface. In the system emulator, a Verilog RTL simulation session corresponding to a specific parameter set can be dynamically loaded at runtime to provide metamorphism by flexible partial parameter-driven RTL model replacement.

## Employment History

2019 – · · · · **Graduate Researcher** in Kyungpook National University.
• *B.S./M.S./Ph.D. integrated student in School of Electronic and Electrical Engineering.*

## Education

2014 – 2019 **B.S. Electronics Engineering** in Kyungpook National University.
• *Early Graduated, and First student enrolled in a B.S./M.S./Ph.D.-integrated course.*

## Awards and Honors

2023 – 2024 **Ph.D. Research Fellowship**, National Research Foundation of Korea (NRF)
• *Acceptance Rate: 330 among 1400 = 23.5%* ($20K/year)

## Research Publications

### Journal Articles

1. **J. Kwon** and D. Park, "Sliding -Window-based Fast and Lightweight ADC Pseudo-Randomness Compensation Technique for Low-Cost ADC", (In preparation).
2. **J. Kwon** and D. Park, "Efficient Partial Weight Update Techniques for Lightweight On-Device Learning on Tiny Flash-Embedded MCUs", *IEEE Embedded Systems Letters*, 2023. DOI: 10.1109/LES.2023.3298731.

3. S. Lee, **J. Kwon**, and D. Park, "Optimized Replication of ADC-Based Particle Counting Algorithm with Reconfigurable Multi-Variables in Pseudo-Supervised Digital Twining of Reference Dust Sensor Systems", *Sensors*, vol. 23, no. 12, 2023, ISSN: 1424-8220. DOI: 10.3390/s23125557.

4. S. Lee, **J. Kwon**, and D. Park, "Runtime Tracking-Based Replication of On-Chip Embedded Software Using Transfer Function Learning for Dust Particle Sensing Systems", *IEEE Access*, vol. 11, pp. 32167–32175, 2023. DOI: 10.1109/ACCESS.2023.3263057.

5. **J. Kwon** and D. Park, "Efficient Sensor Processing Technique Using Kalman Filter-Based Velocity Prediction in Large-Scale Vehicle IoT Application", *IEEE Access*, vol. 10, pp. 116735–116746, 2022. DOI: 10.1109/ACCESS.2022.3215166.

6. **J. Kwon** and D. Park, "Hardware/Software Co-Design for TinyML Voice-Recognition Application on Resource Frugal Edge Devices", *Applied Sciences*, vol. 11, no. 22, 2021, ISSN: 2076-3417. DOI: 10.3390/app112211073.

7. **J. Kwon**, M. G. Seok, and D. Park, "Low-Power Fast Partial Firmware Update Technique of On-Chip Flash Memory for Reliable Embedded IoT Microcontroller", *IEICE Transactions on Electronics*, vol. E104.C, no. 6, pp. 226–236, 2021. DOI: 10.1587/transele.2020LHP0001.

8. **J. Kwon**, M. G. Seok, and D. Park, "GPU-Based ECC Decode Unit for Efficient Massive Data Reception Acceleration", *Journal of Information Processing Systems*, vol. 16, no. 6, pp. 1359–1371, 2020. DOI: 10.3745/JIPS.01.0060.

## Domestic Journal Articles

1. **J. Kwon** and D. Park, "Collaborative Streamlined On-Chip Software Architecture on Heterogenous Multi-Cores for Low-Power Reactive Control in Automotive Embedded Processors", *IEMEK Journal of Embedded Systems and Applications*, vol. 17, no. 6, pp. 375–382, 2022, ISSN: 1424-8220. DOI: 10.14372/IEMEK.2022.17.6.375.

2. J. Baek, J. Jung, M. Kim, **J. Kwon**, and D. Park, "Low-Power Metamorphic MCU using Partial Firmware Update Method for Irregular Target Systems Control", *Journal of the Korea Institute of Information and Communication Engineering*, vol. 25, no. 2, pp. 301–307, 2021, ISSN: 2234-4772. DOI: 10.6109/jkiice.2021.25.2.301.

3. **J. Kwon** and D. Park, "Acceleration of ECC Computation for Robust Massive Data Reception under GPU-based Embedded Systems", *Journal of the Korea Institute of Information and Communication Engineering*, vol. 24, no. 7, pp. 956–962, 2020, ISSN: 2234-4772. DOI: 10.6109/jkiice.2020.24.7.956.

4. **J. Kwon** and D. Park, "Velocity and Distance Estimation-based Sensing Data Collection Interval Control Technique for Vehicle Data-Processing Overhead Reduction", *Journal of the Korea Institute of Information and Communication Engineering*, vol. 24, no. 12, pp. 1697–1703, 2020, ISSN: 2234-4772. DOI: 10.6109/jkiice.2020.24.12.1697.

5. **J. Kwon**, J. Cho, and D. Park, "Efficient Flash Memory Access Power Reduction Techniques for IoT-Driven Rare-Event Logging Application", *IEMEK Journal of Embedded Systems and Applications*, vol. 14, no. 2, pp. 87–96, 2019, ISSN: 1424-8220. DOI: 10.14372/IEMEK.2019.14.2.87.

## Conference Proceedings

1. **J. Kwon** and D. Park, "Efficient Partial Weight Update Techniques for Lightweight On-Device Learning on Tiny Flash-Embedded MCUs", in *ACM SIGBED International Conference on Embedded Software (EMSOFT)*, *Published in *IEEE Embedded Systems Letters*, Hamburg, Germany, Sep. 2023, pp. 1–4. DOI: 10.1109/LES.2023.3298731.

2. **J. Kwon** and D. Park, "Work-in-Progress: Micro-Accelerator-in-the-Loop Framework for MCU Integrated Accelerator Peripheral Fast Prototyping", in *ACM SIGBED International Conference on Embedded Software (EMSOFT)*, Hamburg, Germany, Sep. 2023, pp. 1–2.

3. **J. Kwon**, H. Yun, and D. Park, "Hardware Accelerator Processing Element Unit Dynamic Pruning using Runtime RTL Simulation Reconfiguration", in *2023 International Midwest Symposium on Circuits and Systems (MWSCAS)*, Arizona, USA, Aug. 2023, pp. 1–4.

4. **J. Kwon** and D. Park, "Lightweighted AI-based Inference using Deterministic Randomness Compensation for Microcontroller ADC Resolution Enhancement", in *2022 19th International SoC Design Conference (ISOCC)*, Gangneung, South Korea, Oct. 2022, pp. 368–369. DOI: 10.1109/ISOCC56007.2022.10031497.

5. **J. Kwon**, M. G. Seok, and D. Park, "Neural Network-based Approximate Quality Prediction for Parameter Exploration in Industrial Manufacturing", in *2022 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS)*, Penang, Malaysia, Nov. 2022, pp. 1–4. DOI: 10.1109/ISPACS57703.2022.10082830.

6. **J. Kwon**, S. Oh, and D. Park, "Metamorphic Edge Processor Simulation Framework Using Flexible Runtime Partial Replacement of Software-Embedded Verilog RTL Models", in *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, Daegu, South Korea, May. 2021, pp. 1–5. DOI: 10.1109/ISCAS51556.2021.9401354.

7. **J. Kwon** and D. Park, "Toward Data-Adaptable TinyML Using Model Partial Replacement for Resource Frugal Edge Device", in *The International Conference on High Performance Computing in Asia-Pacific Region (HPC Asia 2021)*, Virtual Event, South Korea: Association for Computing Machinery, Jan. 2021, pp. 133–135. DOI: 10.1145/3432261.3439865.

8. M. Kim, J. Baek, J. Jung, **J. Kwon**, and D. Park, "Segmented Polynomial Approximation for Controlled System Characteristic Estimation on Lightweight Edge Device", in *2020 IEEE International Conference on Consumer Electronics - Asia (ICCE-Asia)*, Seoul, South Korea, Dec. 2020, pp. 1–2. DOI: 10.1109/ICCE-Asia49877.2020.9276901.

9. **J. Kwon** and D. Park, "Efficient Massive Data Reception Using GPU-based ECC Decoding Operation Acceleration", in *2020 World IT Congress (WITC)*, *Recommended to *Journal of Information Processing Systems*, Seoul, South Korea, Feb. 2020, pp. 1–6.

10. **J. Kwon** and D. Park, "Implementation of Computation-Efficient Sensor Network for Kalman Filter-based Intelligent Position-Aware Application", in *2020 International Conference on Artificial Intelligence in Information and Communication (ICAIIC)*, Fukuoka, Japan, Feb. 2020, pp. 565–568. DOI: 10.1109/ICAIIC48513.2020.9065098.

11. **J. Kwon**, M. G. Seok, and D. Park, "User Insensible Sliding Firmware Update Technique for Flash-Area/Time-Cost Reduction toward Low-Power Embedded Software Replacement", in *2020 IEEE Symposium in Low-Power and High-Speed Chips (COOL CHIPS 23)*, Kokubunji, Japan, Apr. 2020, pp. 1–3. DOI: 10.1109/COOLCHIPS49199.2020.9097638.

12. **J. Kwon**, J. Cho, and D. Park, "Efficient Flash Memory Access Power Reduction Techniques for IoT-Driven Rare-Event Logging Application", in *2019 IEEE Symposium in Low-Power and High-Speed Chips (COOL CHIPS 22)*, *Poster Session, Yokohama, Japan, Apr. 2019, pp. 1–2.

13. **J. Kwon**, J. Cho, and D. Park, "Function Block-Based Robust Firmware Update Technique for Additional Flash-Area/Energy-Consumption Overhead Reduction", in *2019 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS)*, Taipei, Taiwan, Dec. 2019, pp. 1–2. DOI: 10.1109/ISPACS48206.2019.8986373.

### Books and Chapters

1. D. Park and **J. Kwon**, *Low-Power Digital System Design – Practical Approach*. TNES Inc., 2021, (Korean), ISBN: 979-11-965255-3-8. URL: https://books.google.co.kr/books?id=_oZOEAAAQBAJ.

## Patents

### South Korea

1. D. Park and **J. Kwon**, "Firmware Update Method using QR Code Image and Electronic Device Performing Same", KR Patent App. 10-2391306, Apr. 2022. URL: https://patents.google.com/patent/KR102391306B1/en.
2. D. Park and **J. Kwon**, "Code Insertion Module and Method for Dividing Storage of Firmware Segment", KR Patent App. 10-2391312, Apr. 2022. URL: https://patents.google.com/patent/KR102391312B1/en.
3. D. Park and **J. Kwon**, "Firmware Update Device and Update Method", KR Patent App. 10-2375290, Mar. 2022. URL: https://patents.google.com/patent/KR20220019940A/en.
4. D. Park and **J. Kwon**, "Memory Connection System and Memory Connection Method for Acceleration of Operation", Pending in Korea Patent and Trademark Office, Dec. 2022.
5. D. Park and **J. Kwon**, "APPARATUS AND METHOD TO UPDATE WEIGHT FOR ON-DEVICE LEARNING OF NEURAL NETWORK MODEL", Pending in Korea Patent and Trademark Office, Nov. 2021.
6. ——, "Self-Reprogramming-based Software Mal-function Fix Method of Firmware Configured by Control Flow and Parameters", Pending in Korea Patent and Trademark Office, Nov. 2021.
7. D. Park and **J. Kwon**, "SYSTEM AND METHOD FOR SIMULATING MICRO ACCELERATOR", Pending in Korea Patent and Trademark Office, Nov. 2021.

## Professional Experiences

### Teaching Assistant

2020 – 2023 **Kyungpook National University**, Daegu, South Korea
- 2020S, *Introduction to Computer Science and Engineering (ITEC201)* for Prof. Hohee Kim.
- 2020S, 2020F, *C Programming (EECS201)* for Prof. Daejin Park.
- 2020W, 2021W, *Logic Circuits (ELEC247)* for Prof. Daejin Park.
- 2021S, 2023S, *Embedded System Design (EECS420)* for Prof. Daejin Park.
- 2023S, *Logic Circuit Design (COMP331)* for Prof. Daejin Park.
- 2023S, *Digital Signal Processing (ELEC701)* for Prof. Daejin Park.

### Projects

2023 – **National Research Foundation of Korea (NRF)**
- *IoT Processor HW/SW Embedded Weight Parameter Intelligence and On-Chip Software Platform for Lightweight Edge AI Computation*

**Institute for Information & communication Technology Planning & evaluation (IITP)**
- *Self Supervised Learnable Flexible AI-Edge Processors*

2022 – **Institute for Information & communication Technology Planning & evaluation (IITP)**
- *Processing-in-Memory (PIM) Semiconductor Design Research Center*

2021
- *Low-Power Sound Interface with Signal Processing $I^2S$ Unit*
- *DSI3 Robust Interface Design for Automotive Connectivity for Ultrasonic Sensor MCU*
- *SENT & SWI Interface Design for Automotive Connectivity for Force Sensor IC*
- *Particle Counting Parameter Exploration Algorithm Design for Dust Sensor IC*

2021 – 2022
- *Embedded IoT Virtualization-based Digital-Twin Smart Fabrication*

2020 – 2021
- *Digital Twin-based Virtual Sensor Synthesis and Intelligent Parameter Optimization*

2020 **Daegu Science High School**, Daegu, South Korea
- *Context-Recognition Intelligent Automatic Control Systems based on Self-Reprogramming*

## Professional Experiences (continued)

2019 – 2022 **National Research Foundation of Korea (NRF)**
• *Re-adaptative Runtime Synthesis and Low-Power Execution Platform of Things-Cloud Connected Software/Hardware for Lightweight Intelligent IoT Device*

## Skills

Languages Korean (Native), English (Intermediate)
Coding C/C++, Verilog, Shell script, Tcl, MATLAB
Tool EDA (Synopsys/Cadence), Xilinx (Vivado, HLS, Vitis), LaTeX, STMicro (STM32CubeIDE)

## Miscellaneous

### Invited Talks

Aug. 2023 **PIM Semiconductor Research Center** in Korea Advanced Institute of Science & Technology (KAIST)
• *Embedded C Programming for PIM Semiconductor*

### Domestic Software Copyrights

Jul. 2023 D. Park and **J. Kwon**, "Singular-Value-Decomposition Program", Korea Copyright Commission. C-2023-031932.

Nov. 2022 D. Park and **J. Kwon**, "Inverse matrix calculation program", Korea Copyright Commission, C-2022-047263.

D. Park and **J. Kwon**, "Manufacturing Quality Prediction Neural Network Training and Inference Program", Korea Copyright Commission, C-2022-047264.

D. Park and **J. Kwon**, "Multi-core Collaborative Digital Signal Distributed Processing Program", Korea Copyright Commission, C-2022-047989.

Nov. 2021 D. Park and **J. Kwon**, "Embedded System Firmware Partial Update Program", Korea Copyright Commission [C-2021-043262.

D. Park and **J. Kwon**, "Atypical Sensor ADC Data Compensate Dust Particle PM Calculating Binary Firmware", Korea Copyright Commission, C-2021-043261.

Last updated: October 23, 2023