

Joonghyun An

ELECTRONICS ENGINEER · HARDWARE

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Bio Sketch

Mr. An received the M.S. degree in School of Electronics Engineering from Kyungpook National University, Daegu, Korea, in 2017. His research interests include ultra-low power VLSI chip design for IoT-driven applications and implementing machine learning. He has a lot of experience in the design of SoC(System on Chip) for embedded systems such as MCUs, and has published several journal/conference papers related robust processor architecture protecting abnormal clock failure. He had developed ARM-based NAND flash controllers with Custom-Designed VLSI circuits at SK Hynix Semiconductor. Currently, He is developing the storage interface part of the Mobile AP(Application Processor) for Samsung Electronics' flagship products at Samsung Semiconductor and is researching the theory of DSP(Digital Signal Processing) for artificial intelligence development for self-improvement.

Education

Chungbuk National University

B.S. IN ELECTRONICS ENGINEERING

Cheongju, S.Korea

Mar. 2000 – Feb. 2007

Kyungpook National University

M.S. IN ELECTRONICS ENGINEERING

Daegu, S.Korea

Mar. 2015 – Feb. 2017

Kyungpook National University

PH.D CANDIDATE IN ELECTRONICS ENGINEERING

Daegu, S.Korea

Mar. 2022 – Present

Skills

Programming Embedded C, Verilog HDL, C-shell, Tcl, Perl

Tool NCVerilog, VCS, Simvision, Verdi, Design Compiler, Prime Time, Formality, Vivado, Altera

Languages Korean, English

Publications

JOURNAL PUBLICATIONS

Automatic On-Chip Glitch-Free Backup Clock Changing Method for MCU Clock Failure Protection in Unsafe I/O Pin Noisy Environment

JOONGHYUN AN, JIAE YOUN, JEONGHUN CHO, DAEJIN PARK

Journal of The Institute of Electronics and Information Engineers(KCI)

2015

Safe Adaptive Headlight Controller with Symmetric Angle Sensor Compensator Using Steering-Swivel Angle Lookup Table

JIAE YOUN, JOONGHYUN AN, MENG DI YIN, JEONGHUN CHO, DAEJIN PARK

Transactions of the Korean Society of Automotive Engineers(KCI)

2016

Automatic On-Chip Backup Clock Changer for Protecting Abnormal MCU Operations in Unsafe Clock Frequency

JOONGHYUN AN, MOON GI SEOK, DAEJIN PARK

IEICE Electronics Express(SCI)

2016

Fast Adaptation Techniques of Compensation Coefficient of Active Noise Canceller using Binary Search Algorithm

JOONGHYUN AN, DAEJIN PARK

*Journal of the Korea Institute of
Information and Communication
Engineering(KCI)*

2021

CONFERENCE PUBLICATIONS

On-Chip Glitch-Free Backup Clock Changer using Noise Canceller and Edge Detector for Automatic MCU Clock Failure Protection

2015 ISET

JOONGHYUN AN, DAEJIN PARK

2015

On-chip Glitch-Free Backup Clock Changer with Noise Canceller and Edge Detector for Safety MCU Clock System

*2015 IEEE 4th Global Conference on
Consumer Electronics (GCCE)*

JOONGHYUN AN, JEONGHUN CHO, DAEJIN PARK

2015

Safe Microcontroller with On-Chip Bus Transition Monitor and Glitch-Free Backup Clock Changer for Clock-Failure Protection

2016 IEEE COOLChips

JOONGHYUN AN, DAEJIN PARK

2016

Acoustic Event Detection-Based Individualized Things-Human Interaction using Matlab-Microcontroller Interoperation

*2016 IEEE 5th Global Conference on
Consumer Electronics*

SEONG SEOP KIM, JOONGHYUN AN, JEONGHUN CHO, DAEJIN PARK

2016

Runtime Compensation Coefficient Estimation Techniques using Binary Search Algorithm for Low-Power Active Noise Cancelling Systems

2021 IEEE ICCE-Asia

JOONGHYUN AN, DAEJIN PARK

2021

Projects

Embedded Flash+EEPROM Combi General Micocontroller with Common Function

ABOV Semiconductor, S.Korea

SoC DESIGN

Jan. 2007 – Aug. 2008

- Peripheral Design and Verification
- Synthesis, Static Timing Analysis
- FPGA Verification using altera cyclone series

Embedded Flash+EEPROM Combi Micocontroller with ROM Encryption

ABOV Semiconductor, S.Korea

SoC DESIGN

Nov. 2008 – May. 2009

- System Interface Design and Verification
- Wafer/PKG test setup

HDMI-CEC Compliant Microcontroller Design

ABOV Semiconductor, S.Korea

SoC DESIGN

Aug. 2009 – Jan. 2010

- IP Design for dual graphic interface chip for display processor

Dedicated Microcontroller for LED BLU control

ABOV Semiconductor, S.Korea

SoC DESIGN

Mar. 2010 – Dec. 2012

- BLU(Back Light Unit) control IP Design and Verification
- Mass production follow up

Flash Control device with UFS 2.0 host protocol

SK Hynix, S.Korea

SoC DESIGN

Mar. 2013 – May. 2014

- NAND Flash control IP Design and Verification

Flash Control device with eMMC 5.1 host protocol

SK Hynix, S.Korea

SoC DESIGN

Aug. 2014 – May. 2016

- NAND Flash control IP Design and Verification

Flash Control device with UFS 3.0/2.1 Combi host protocol

SoC DESIGN

- Cortex-M3 core Integration and Verification

SK Hynix, S.Korea

Sep. 2016 – Jun. 2018

Flash Control device with UFS 4.0 host protocol

SoC DESIGN

- NAND PHY IP design for high speed NAND Flash access

SK Hynix, S.Korea

Jan. 2020 – Dec. 2022

Mobile AP(Application Processor) design for flagship product

SoC DESIGN

- UFS 4.1 host protocol based Storage Interface

Samsung Semiconductor, S.Korea

Jul. 2023 – Present