GihyeonJeon

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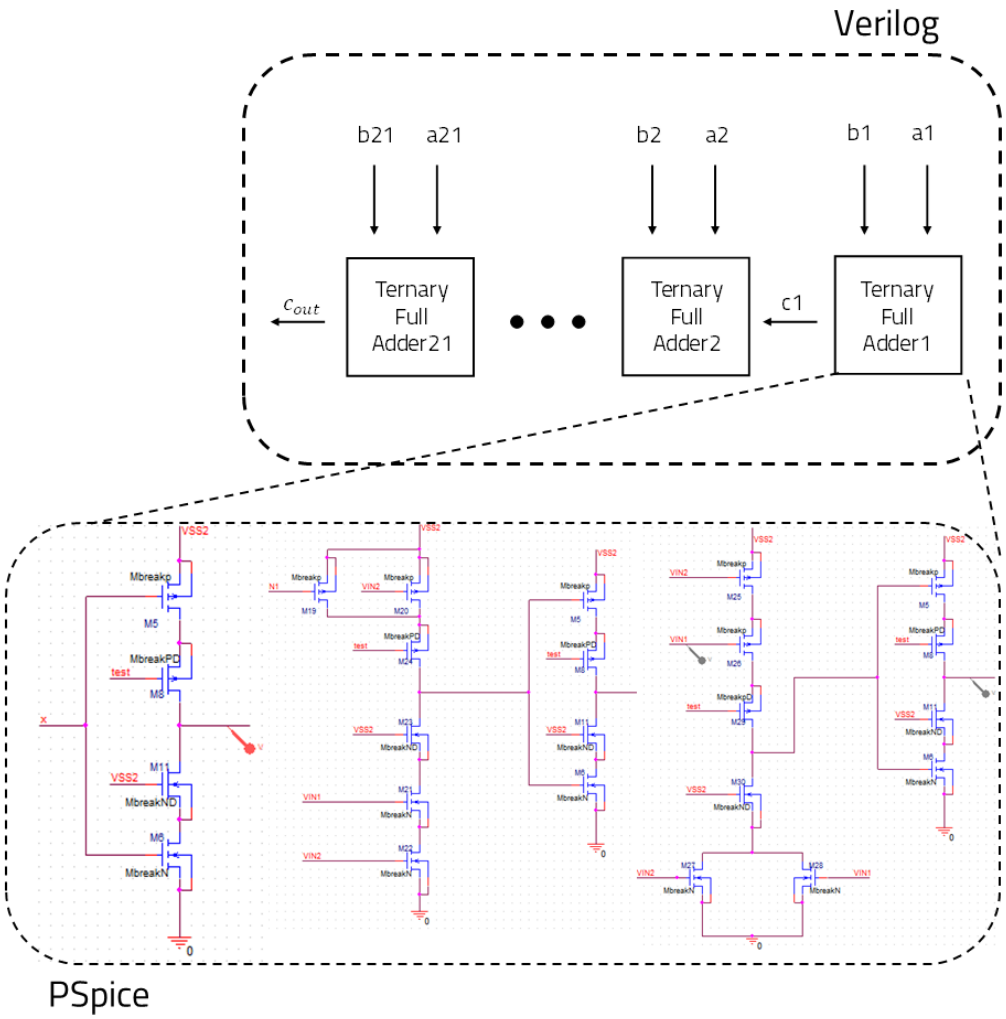
EDUCATION

KyungPook National University | *Master's Degree* **2024**

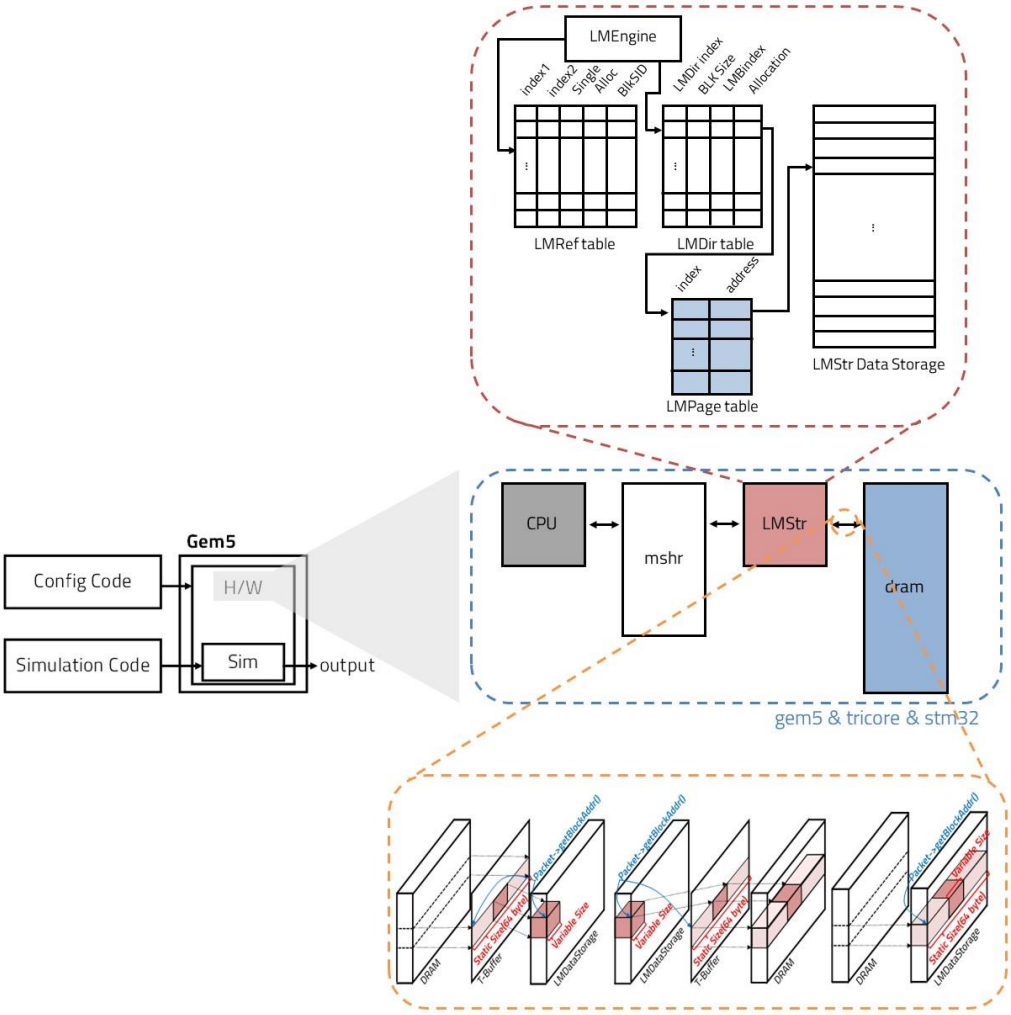
- 2020 - 2024 | B.S. in School of Electronics Engineering
- 2024 - | M.S. in School of Electronics Engineering

RESEARCH INTERESTS 1



- With the rapid advancement of artificial intelligence and AI technologies, there has been a significant increase in operational workloads. Consequently, there is a need to handle these increased workloads within a fixed and precise timeframe. Anticipating that representing large numbers with fewer digits could increase operation speed, I constructed ternary logic gates and used them to create a ternary ripple carry adder. To construct this system, I employed Verilog RTL simulation and PSpice simulation. In PSpice, I designed each logic gate and measured their delay times. Using Verilog VPI, I conducted an overall performance comparison of the adders. The results confirmed that the designed ternary ripple carry adder exhibited approximately 75% better performance compared to the binary ripple carry adder. Due to the faster operation speed, I assumed that there would be a range where energy consumption is more advantageous and calculated that range. In the future, I plan to leave room for further work, such as designing layouts or researching ternary logic gates that do not follow the conventional form of binary logic gates.

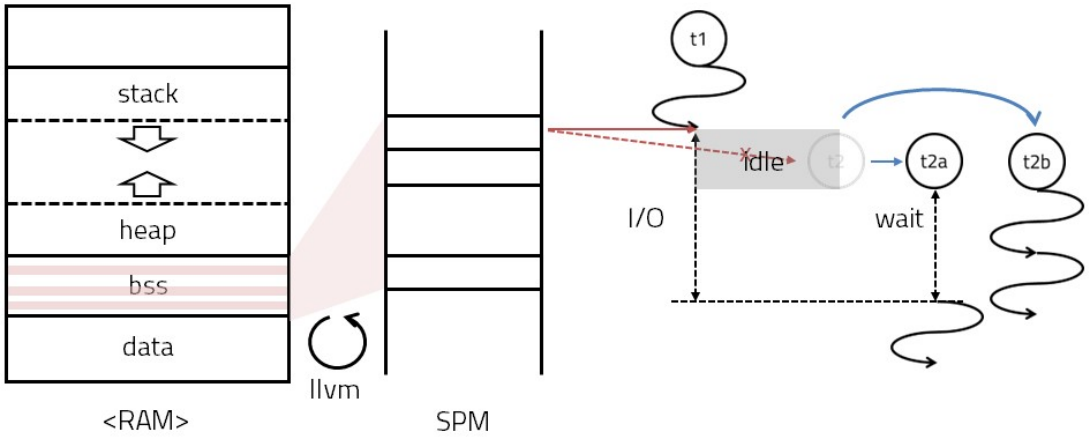
RESEARCH INTERESTS 2



- Cache memory, being controlled by hardware, incurs significant hardware burden and power consumption. This led to the emergence of scratchpad memory. However, scratchpad memory, being software-controlled, increases the burden on programmers and compilers. Therefore, the use of scratchpad memory based on local memory store (LMStr) has been proposed to reduce the burden on programmers and compilers due to conventional scratchpad memory. However, this structure cannot be free

from the fragmentation problem due to storing variable block sizes in the data storage space. As a method to use the same memory space more efficiently, I propose an LMStr structure that applies paging. This structure stores data blocks of a fixed size, not variable size, thus it is free from external fragmentation and has a higher hit ratio due to data locality. And the proposed structure is tested in the gem5 simulation environment. To simulate this structure in gem5, a new structure that does not affect the results of the simulation enables this and allows obtaining the desired outcomes.

RESEARCH INTERESTS 3 (ON-GOING)



- Use llvm to allocate frequently used global variables to scratchpad memory. And in multi-threads, scratchpad memory is treated as shared memory. This is a study to solve memory problems that may occur at this time.

EXPERIENCE

Teaching Assistant

- 2024S, Microprocessor Design Experiment for Prof. Daejin Park
- 2024S, Embedded Linux Lecture of **Hyundai Autoever** for Prof. Daegin Park
- 2024S, Microprocessor & Embedded Linux Lecture of **LIGNex1** for Prof. Daejin Park

PROJECTS

Typora: Auto Upload GitHub to avoid duplicate file names | *GitHub Link*

- Due to Picgo's problem, files with duplicate names are not registered on GitHub.
- Therefore, the problem was solved by having the time stamp registered in the file name through script.

PARTICIPATION IN INTERNATIONAL CONFERENCE

2023 IEMEK Fall Conference 2023, Jeju, Korea

2023 IEEE ICMU 2023, Kyoto, Korea

2024 IEEE ICEIC 2024, Taipei, Taiwan

2024 IEEE COOLChips 2024, Tokyo, Japan